ISO-9001
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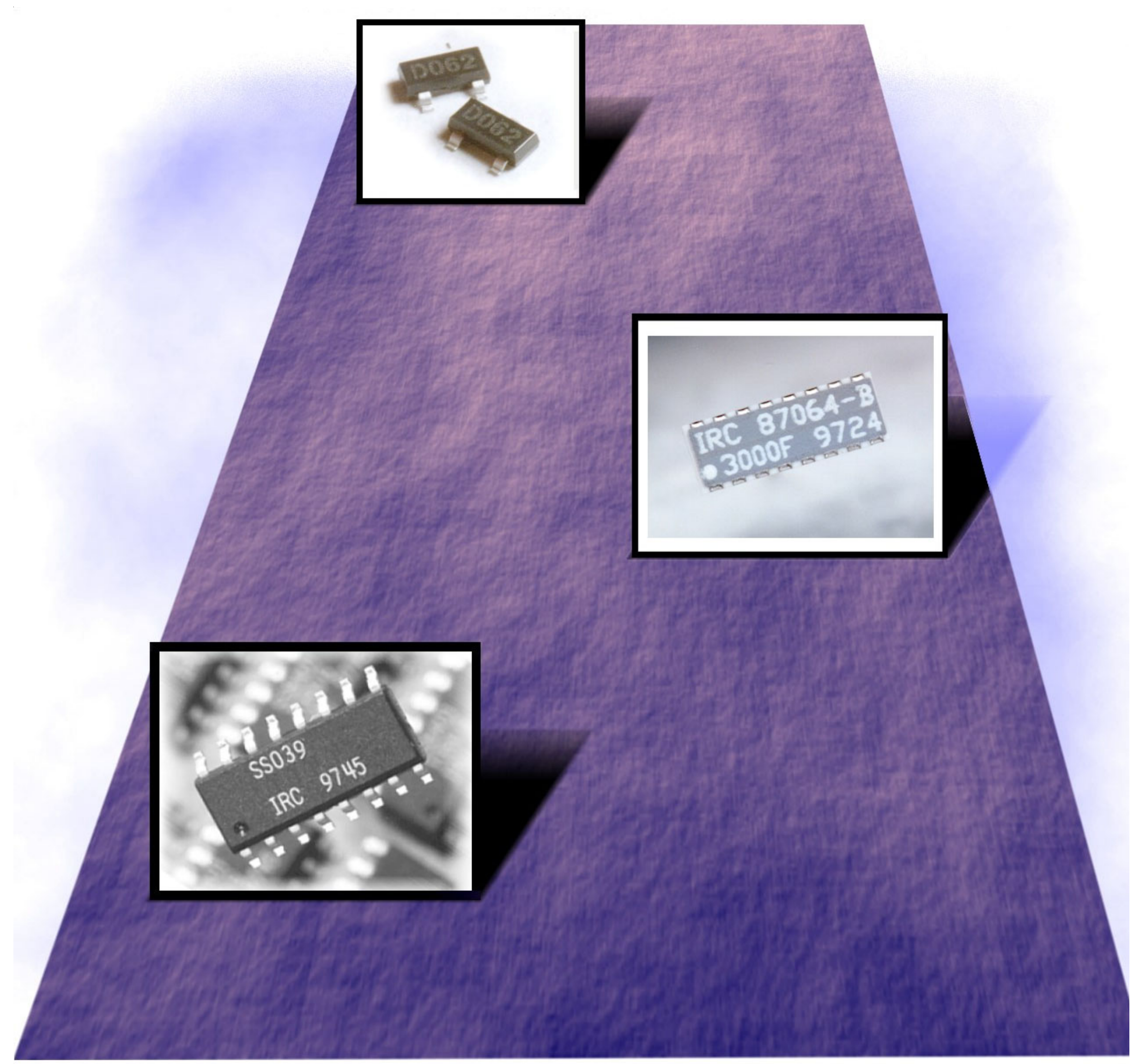
Application Note AFD005

CERAMIC OR SILICON?



Contact:

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References:

- PFC Divider (D1206) Data Sheet
- SOT23 Data Sheet
- SON Series Data Sheet
- SOIC Series Data Sheet

APPLICATION NOTE IRC/AFD005

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Issue

What is the best substrate for a resistor network? Traditionally, the most popular substrate for resistor networks has been ceramic, but recently passive component manufacturers have begun to produce resistor networks on silicon substrates. What are the advantages and disadvantages of each of these materials? In what situations does an application call for ceramic? For silicon?

Discussion

Ceramic Substrates

Ceramic provides a rigid, stable surface with superb dielectric strength and very good high frequency performance. Ceramic-based resistor networks can be manufactured to exacting tolerances and exhibit superb stability over life due to the robust package design and the ability to “trim out” resistance shifts that are created as a by-product of the resistor network assembly.

High purity (99.5% or 99.6%) alumina substrates are used in the construction of thin film resistor networks. A .025” thick ceramic die forms an inflexible platform that is resistant to the strain gauge effects associated with molded type packages. Mold compounds can impart large local stresses on resistor elements during the curing process. These stresses in turn cause a bending moment on the resistor die and the resistor elements contained thereon resulting in a positive or negative resistance shift depending on which direction the die is deflected. IRC’s ceramic packages are constructed using the ceramic resistor substrate as the package itself (figure 1).

Figure 1. Ceramic Substrate Package

The resistor network is encapsulated using a screen-printed epoxy or ceramic lid resulting in a resistor package which does not have the strain effects associated with molded encapsulation.

A process flow diagram for ceramic-based resistors is shown in figure 2. There are very few process stresses on the resistive elements that would cause a change in the resistance tolerance after the final laser adjust. Operations which cause small resistance shifts such as lead attach can be performed before the resistor elements receive final adjustment. In this case, any shift in resistance due to the lead attach operation is compensated for at a final laser adjust.

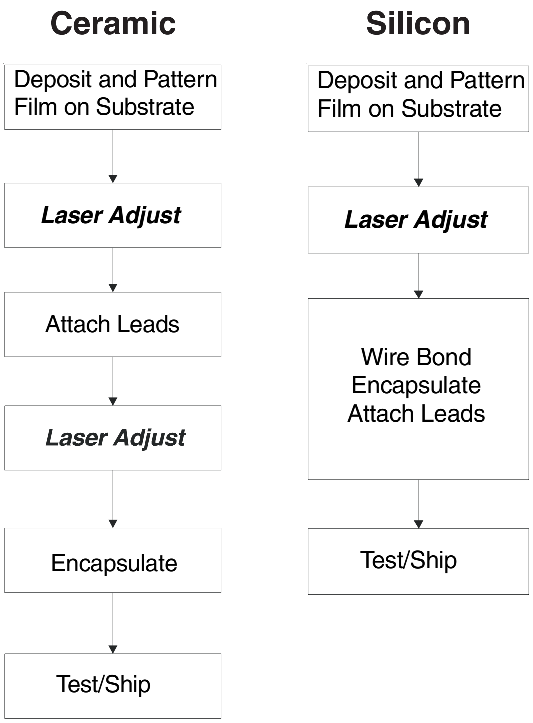

Figure 2. Ceramic and Silicon Process Flow

Silicon Substrates

Resistor networks constructed with silicon substrates are very economical to produce in large quantities because the smaller geometries that can be accomplished on silicon permit the design of smaller dice and thus more dice per substrate. Resistor networks constructed on silicon substrates are packaged in wire bonded, molded packages such as SOT, SOIC, QSOP and TSSOP packages (see figure 3). These packages have become very popular due to inexpensive assembly costs and the influence of the semiconductor industry, where these packages are widely sold. Circuit designers often wish to specify these popular, standard packages for all of their resistor network needs – including those requiring tight tolerances and high stability. But silicon based devices are not the best choice for high performance applications requiring tight tolerances and/or high stability.

When the silicon die is molded into an epoxy package, the mold compound places stress on the die containing the resistive elements causing small shifts in the resistance of the network elements. These shifts cannot be compensated for at laser trim since the device is already encapsulated. There is no opportunity for subsequent resistor adjustment after the first and only laser adjustment (figure 2). Resistance shifts occurring after encapsulation require resistor manufacturers to offer these devices at looser specified tolerances and stabilities.

Table 1
Electrical Performance, Ceramic vs. Silicon

Characteristic	**Ceramic**	**Silicon**
Resistance Range	0.5S to 1 MegS	5S to 500KS
Absolute Tolerance	To ±0.02%	To ±0.1%
Ratio Tolerance	To ±0.01%	To ±0.05%
Absolute TCR	To ±10 ppm/°C-Chips To ±15 ppm/°C-Networks	To ±25 ppm/°C
TCR Tracking	To ±1 ppm/°C	To ±2 ppm/°C
Noise	< -30db	< -30db
TCR Linearity	< ±2 ppm	< ±2 ppm

Table I compares the electrical performance of equivalent resistor networks constructed on silicon and ceramic substrates. The values shown are representative of a resistor network optimized for performance; i.e. mid-range values, ratio tracking between like-value pairs, close proximity resistors.

Solutions:

The problem is achieving ceramic performance in the same footprint as a silicon-based package. One way to solve the problem is to provide ceramic-based packages that match or nearly match the footprints of popular silicon-based packages.

SOIC – SON IRC manufactures narrow SOIC packages using silicon substrates for applications requiring tolerances to ±0.1%. For tolerances from ±0.1% to ±0.01%, IRC offers the ceramic SON package which can be used on the same PC board layout as the SOIC package. The SON was designed specifically to match the land pads used for a narrow SOIC package as shown in Figure 6. With the SON device, circuit designers have the option to use either a silicon based SOIC (for medium to loose tolerance applications) or a ceramic based SON (for tight tolerance applications) on the same PC board design.

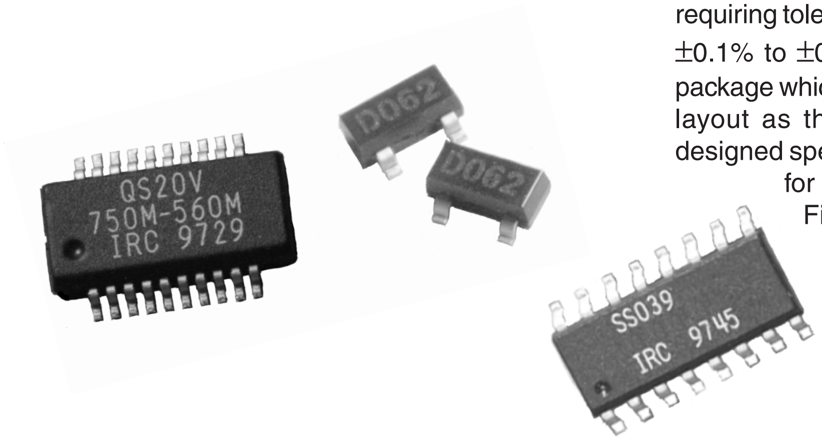

Figure 3. QSOP, SOT23, and SOIC Packages.

SOT23 - PFC DIVIDER IRC manufactures silicon-based SOT23 devices (figure 4) containing two resistors in a voltage divider configuration. This device is available for applications to ±0.05% with ±2ppm/°C TCR tracking. For applications requiring tolerances from ±0.05% to ±0.01%, IRC offers the PFC divider package (figure 5). Although not an exact drop in replacement for the SOT23 package, the PFC divider pad layout can be easily combined with the SOT23 pad layout as shown in figure 7. Circuit designers then have the option to use a highly stable device such as the PFC divider *or* the SOT23 without a redesign of the PC board.

Summary:

Use ***Ceramic*** Based Packages for:
- Tight Tolerance
- Tight TCR
- Excellent Stability

Use ***Silicon*** Based Packages for:
- Good Stability
- High Volume
- High Density
- Low Cost

For more information on ceramic or silicon based devices or to discuss your particular application, check out the IRC web site at http://www.irctt.com or contact the factory at 512-992-7900.

Figure 4. SOT23 Device

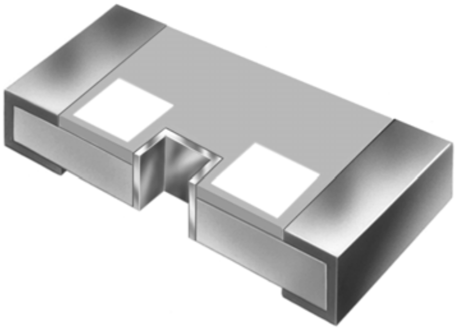

Figure 5. PFC Divider Package

0.150" SOIC Land Pattern per IPC-SM-782 Rev A

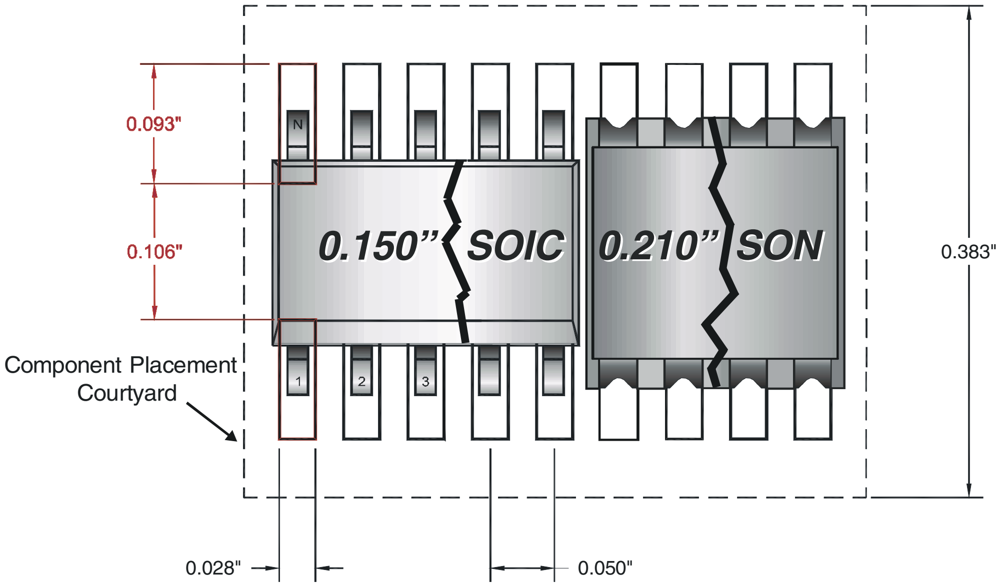

Figure 6. Land Pad layout for SOIC/SON Divices.

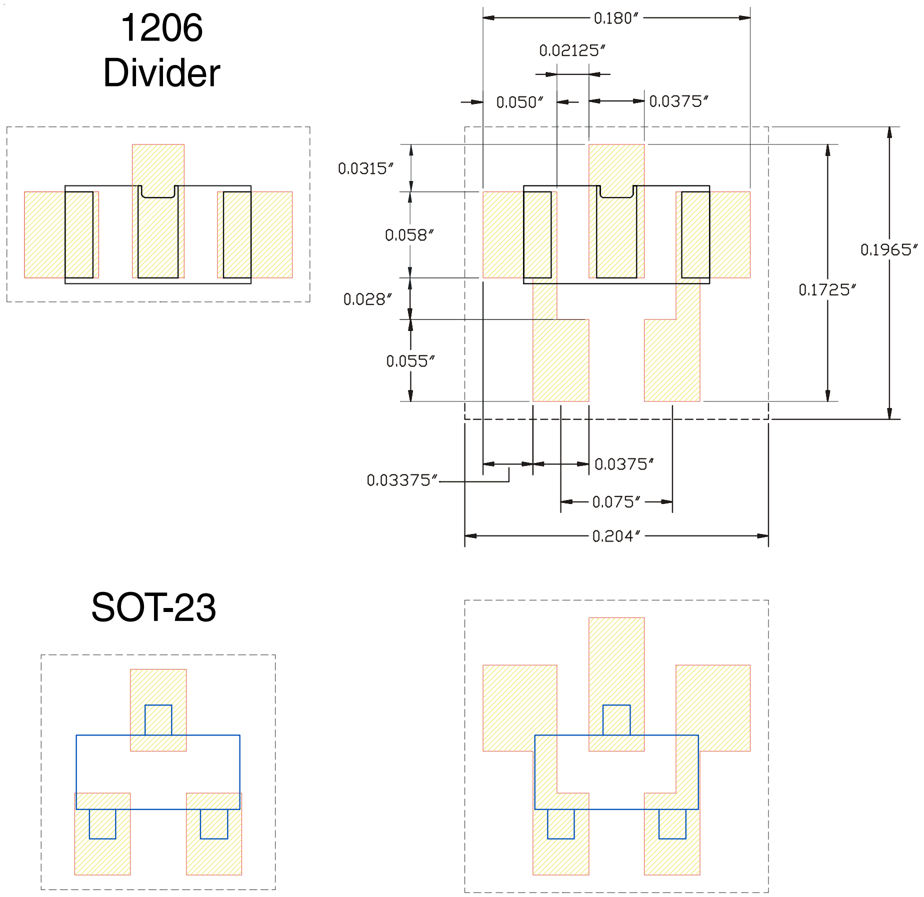

Figure 7. Combination Pad layout for PFC Divider and SOT23