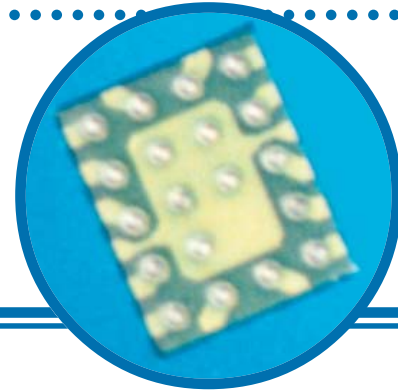


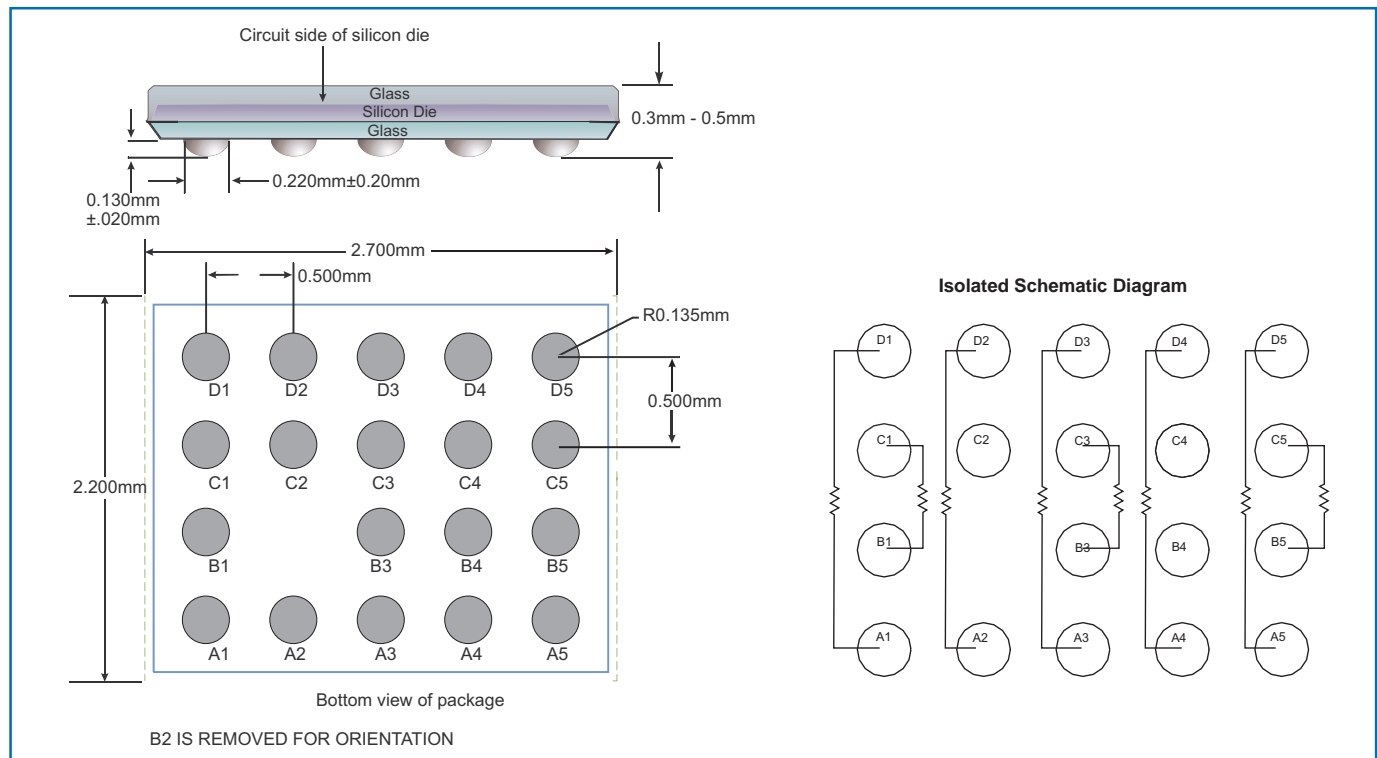
Chipscale Termination Array

- Wafer level processing
- Thin film on silicon technology
- Excellent solution for thin, portable products
- Compliant and reworkable - No underfill required



IRC now offers wafer level packaged components integrating tantalum nitride resistors in an application specific circuit. Based on IRC's proven TaNSi[®] Technology, high density packages are available to suit the most demanding high density applications. IRC's wafer level packaging offers smaller sizes than traditional SOIC and QSOP packages while still offering solder bump or compliant lead connections.

Outline Dimensions and Schematic Diagram



General Note

IRC reserves the right to make changes in product specification without notice or liability. All information is subject to IRC's own data and is considered accurate at time of going to print.

Chipscale Termination Array



Electrical Data

Absolute Tolerance	Absolute TCR	Tracking TCR	Element Power Rating	Package Power Rating	Operating Temperature	Voltage Rating
to $\pm 1\%$	$\pm 250\text{ppm}/^\circ\text{C}$	$\pm 10\text{ppm}/^\circ\text{C}$	100mW	500mW	-40°C to $+85^\circ\text{C}$	50V

Ordering Procedure

Prefix **CHS** - **SD0550A** - **01** - **51R0** - **J**

Model
4 X 5 array, isolated schematic

Absolute TCR Code
99 = $250\text{ppm}/^\circ\text{C}$

Four Digit Resistance Code
Standard Resistance Values
22R0 = 22S; 33R0 = 33S; 47R0 = 47S; 50R0 = 50S
51R1 = 51S; 75R0 = 75S; 1000 = 100S

Absolute Tolerance Code
J = $\pm 5\%$; F = $\pm 1\%$

For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.