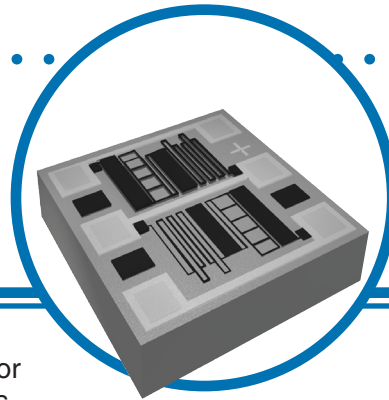


# Wire Bondable Chip Resistors



## WBC Series

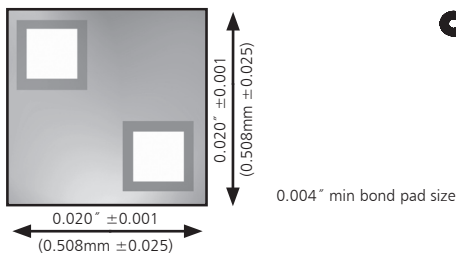
- Discrete or tapped schematics
- MIL inspection available
- High resistor density

IRC's WBC series wire bondable chip resistors are ideally suited for the most demanding hybrid application. The WBC combines IRC's TaNSil® tantalum nitride thin film technology with silicon substrate processing to produce an extremely small footprint device with the proven stability, reliability and moisture performance of IRC's TaNSil® resistor film.

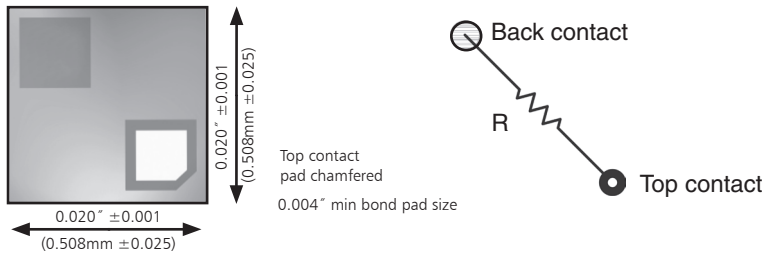
Available in a wide range of tolerances and temperature coefficients to fit a variety of hybrid circuit applications. Custom resistance values, sizes and schematics are available on request from the factory.

## Physical Data

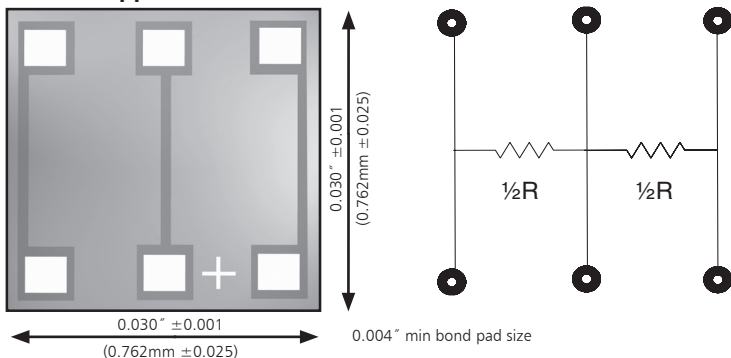
### R0202 - Discrete



### B0202 - Discrete back contact



### T0303 - Tapped network 1/2R + 1/2R



## Electrical Data

<b>Absolute Tolerance</b>	to ±0.1%	
<b>Absolute TCR</b>	to ±25ppm/°C	
<b>Package Power Rating (@ 70°C)</b>	250mW	
<b>Rated Operating Voltage (not to exceed P x R)</b>	100V	
<b>Operating Temperature</b>	-55°C to +150°C	
<b>Noise</b>	<-30dB	
<b>Substrate Material</b>	Oxidized Silicon (10KÅ SiO <sub>2</sub> min)	
<b>Substrate Thickness</b>	0.010" ± 0.001 (0.254mm ± 0.025)	
<b>Bond Pad Metallization</b>	Aluminum	10KÅ minimum
	Gold	15KÅ minimum
<b>Backside</b>	R0202 and T0303	Silicon (Al / Au optional)
	B0202	3KÅ Au minimum 10KÅ Al minimum
<b>Passivation</b>	Silicon Dioxide or Silicon Nitride	

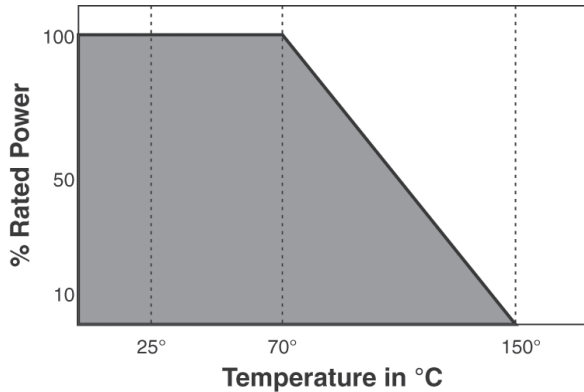
### General Note

IRC reserves the right to make changes in product specification without notice or liability. All information is subject to IRC's own data and is considered accurate at time of going to print.

# Wire Bondable Chip Resistors



## Power Derating Data



## TCR/Inspection Code Table

Absolute TCR	Commercial Code	MIL Inspection Code*
±300ppm/°C	00	04
±100ppm/°C	01	05
±50ppm/°C	02	06
±25ppm/°C	03	07

\*Notes: Product supplied to Class H of MIL-PRF 38534 includes 100% visual inspection

## Manufacturing Capabilities Data

Resistance Range	Available Absolute Tolerances	Available Ratio Tolerances (T0303 only)	Best Absolute TCR	Tracking TCR (T0303 only)
10Ω - 20Ω	G J K	F G J	±100ppm/°C	±50ppm/°C
21Ω - 50Ω	F G J K	F G J	±100ppm/°C	±50ppm/°C
51Ω - 100Ω	C D F G J K	C D F G J	±100ppm/°C	±25ppm/°C
101Ω - 200Ω	C D F G J K	C D F G J	±50ppm/°C	±10ppm/°C
201Ω - 500Ω	B C D F G J K	B C D F G J	±50ppm/°C	±5ppm/°C
501Ω - 999Ω	B C D F G J K	B C D F G J	±25ppm/°C	±2ppm/°C
1.0KΩ - 1.0MΩ	B C D F G J K	A B C D F G J	±25ppm/°C	±2ppm/°C

# Wire Bondable Chip Resistors



## Environmental Data

Test	Method	Max $\Delta R$	Typical $\Delta R$
Thermal Shock	MIL-STD-202 Method 107 Test condition F	$\pm 0.1\%$	$\pm 0.02\%$
High Temperature Exposure	MIL-STD-883 Method 1008 150°C, 1000 hours	$\pm 0.1\%$	$\pm 0.05\%$
Low Temperature Storage	-55°C, 1000 hours	$\pm 0.03\%$	$\pm 0.01\%$
Life	MIL-STD-202 Method 108 70°C, 1000 hours	$\pm 0.5\%$	$\pm 0.01\%$
Life at Elevated Temperature	MIL-STD-202 Method 108 125°C, 1000 hours	$\pm 0.5\%$	$\pm 0.05\%$

## Ordering Data

Prefix ..... **WBC** - **R0202** **A** **S** - **01** - **1002** - **F** **B**

**Style** .....  
 R0202 = Discrete Element  
 B0202 = Discrete Element with Back Contact  
 T0303 = Tapped Network

**Bonding pads** .....  
 A = Aluminum; G = Gold

**Backside** .....  
 A = Aluminum; G = Gold; S = Silicon

**TCR/Inspection Code** .....  
 Reference TCR/Inspection Code Table

**Total Resistance (R)** .....  
 4-Digit Resistance Code Ex: 1002 = 10K $\Omega$ ; 50R1 = 50.1 $\Omega$

**Absolute Tolerance Code** .....  
 K =  $\pm 10\%$ ; J =  $\pm 5\%$ ; G =  $\pm 2\%$ ; F =  $\pm 1\%$ ; D =  $\pm 0.5\%$ ; C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$

**Ratio Tolerance Code (T0303 Only)** .....  
 J =  $\pm 5\%$ ; G =  $\pm 2\%$ ; F =  $\pm 1\%$ ; D = 0.5%; C =  $\pm 0.25\%$ ; B =  $\pm 0.1\%$ ; A =  $\pm 0.05\%$

**Packaging**  
 Standard packaging is 2" x 2" chip tray. For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.